ABSTRACT OF THE DISCLOSURE

The conventional multi-port cache memory, which is formed by using multi-port cell blocks, is excellent in its operating speed. However, the integration area of the constituent multi-port cell blocks is increased in proportion to the square of the number of ports. Thus, if it is intended to decrease the cache miss probability by increasing the storage capacity, the chip size is increased correspondingly, which increases the manufacturing cost. On the other hand, the multi-port cache memory of the present invention is formed by using, as constituents, one-port cell blocks adapted for a large storage capacity, making it possible to easily provide a multi-port cache memory of a large storage capacity and reduced integration area, which has a large random access bandwidth, is capable of parallel access from a plurality of ports, and is adapted for use in advanced microprocessors having a small cache miss probability.